REMARKS

The above amendment along with the following remarks are being submitted as a full and complete response to the Official Action dated February 12, 2003, the period for response expiring June 12, 2003.

Claims 1-14 are under consideration in this application. Claims 15-16 are being cancelled without prejudice or disclaimer. The specification and Fig. 4 are being amended for clarification. Applicant hereby submits that no new matter is being introduced into the application through the submission of this response.

In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Formality Rejection

The specification and figures are objected for some informalities. As indicated, the specification and Fig. 4 are being amended for clarification. Accordingly, the withdrawal of the outstanding informality rejection is in order, and is therefore respectfully solicited.

Prior Art Rejection

Claims 1-6 were rejected under 35 U.S.C. § 103(a) as being unpatentable over JP Pat. No. 04-168417 to Takahara et al. (hereinafter "Takahara"). Furthermore, claims 7-14 were rejected as being unpatentable over Takahara in view of U.S. Pat. No. 6,424,328 B1 to Ino et al. (hereinafter "Ino"). In addition, the Examiner rejected claims 15-16 as being unpatentable over U.S. Pat. No. 5,793,345 to Silverbrook (hereinafter "Silverbrook") in view of U.S. Pat. No. 6,348,909 B1 to Kim (hereinafter "Kim"). The prior art references of Hirai et al. (5,874,933), Nakajima et al. (6,157,358), Koyama et al. (6,380,919 B1), and Aoki et al. (6,025,835) were cited as being pertinent to the present application. These rejections have been carefully considered, but are most respectfully traversed.

The liquid crystal display device of the invention, as now recited in claims 1-2,

comprises: a liquid crystal display element; a plurality of driving circuits; and a display control device transmitting display data including an ineffective datum to the plurality of driving circuits, wherein the display control device transmits a datum having **a same level** as that of an effective display datum being transmitted prior to (claim 1) or subsequently to (claim 2) the ineffective display datum thereby instead of the ineffective display datum during a period when the ineffective display datum should be transmitted thereby.

The present invention, as now recited in claims 3-4, is also directed to a liquid crystal display device comprising: a liquid crystal display element; a plurality of driving circuits; and a display control device transmitting display data for *odd/even numbered* ones of the plurality of driving circuits and display data for *even/odd numbered* ones thereof alternately thereto, wherein the display control device transmits a datum having **a same level** as that of an effective display datum for the *odd/even numbered* one of the plurality of driving circuits being transmitted prior to (claim 3) or subsequently to (claim 4) the ineffective display datum to be inputted to an at least one of the *even/odd numbered* ones thereof instead of the ineffective display datum during a period when the ineffective display datum should be transmitted to the at least one of the *even/odd numbered* ones thereof.

Takahara merely discloses an effective display datum being transmitted prior to the ineffective display datum **"as is"** since "the excess output bits of the driver IC are connected to the auxiliary terminals in which other ends are open (page 8, lines 6-7)." As "i*n the prior art, a high level (referred to simply as H level, hereinafter) or a low level (referred to simply as L level, hereinafter) is outputted as the ineffective display data. However, in this prior art method, there have been some case where as an arrangement of data on the bus line on which the display data is transmitted, there occur, for instance, a repetition of an H-level* ***ineffective*** *display datum -> an L-level* ***effective*** *display datum -> an H-level* ***ineffective*** *display datum, or a repetition of an L-level* ***ineffective*** *display datum -> an H-level* ***effective*** *display datum -> an L-level* ***ineffective*** *display datum, so that the transmission frequency on the bus line increases* (page 3, lines 6-18)". On the other hand, according to the invention," *since a level of the display data is kept away from being altered (changed) during displaying data transmission including ineffective datum from the display control device to each of the driving circuits, transmission frequency on a bus line can be reduced*" (page 11, lines 13-17).

Takahara merely discloses an effective display datum being transmitted prior to the ineffective display datum **"as is"** since "the excess output bits of the driver IC are connected to

the auxiliary terminals in which other ends are open (page 8, lines 6-7)." Takahara not only fails to disclose "**substituting** the ineffective display datum **with** a datum having **a same level** as that of an effective display datum being transmitted prior to or subsequently to the ineffective display datum (claims 1-6)," but also teaches away from the invention by ignoring the datum level for open pins (as admitted by the Examiner on page 3, line 5 of the outstanding office action). One major object of the invention is to reduce the transmission frequency on the bus line of a liquid crystal display device while display data containing ineffective display data are being transmitted from a display control device to a driving circuit in the liquid crystal display device. Takahara simply does not disclose the same-level feature for accomplishing the major object of the invention.

Contrary to the Examiner's allegation that applicants failed to show the criticality of the same-level feature, the above-references portions of the specification evidence the importance of the same-level feature.

The present invention, as now recited in claims 7 and 10, is also directed to a liquid crystal display device comprising: a liquid crystal display element; a plurality of driving circuits; and a display control device transmitting display data inputted for odd numbered ones of the plurality of driving circuits and display data for even numbered ones thereof alternately thereto, wherein the display control device has a first storing means for storing display data for the odd numbered ones of the plurality of driving circuits which are inputted from an outside of the liquid crystal display device and a second storing means for storing display data for the even numbered ones of the plurality of driving circuits which are inputted from an outside of the liquid crystal display device, reads out the display data from the first storing means and the second storing means alternately, and transmits them to the plurality of driving circuits, and wherein the display control device transmits **an effective display datum** for the *odd numbered* ones thereof being transmitted prior to (claim 7) or subsequently to (claim 10) **an ineffective display datum** to be inputted to an at least one of the *even numbered* ones thereof instead of the ineffective display datum during a period when the ineffective display datum should be transmitted to the at least one of the even numbered ones thereof.

As mentioned, Takahara merely discloses an effective display datum being transmitted prior to the ineffective display datum **"as is"** since "the excess output bits of the driver IC are connected to the auxiliary terminals in which other ends are open (page 8, lines 6-7)." Takahara fails to teach directly "**substituting** an ineffective display datum to be inputted to an at least one

of the *even numbered* driving circuits **with** an effective display datum for the *odd numbered* driving circuits being transmitted prior to or subsequently to the ineffective display datum (claims 7-14)."

Ino does not compensate for Takahara's deficiencies. Ino merely discloses dot inversion driving liquid crystal display device, in which a time-division number is set to an odd number when time-division driving is applied to an active-matrix LCD apparatus and time-sequential signal output from the driver IC is time-divided by a time-division switch and sent to signal lines 12-1, 12-2,...to implement complete dot inversion driving (see ABSTRACT).

Accordingly, the present invention as now recited in all the claims is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicant respectfully contends that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of

the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and phone number indicated below.

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In Fig. 5, reference numeral 153 denotes the shift register circuit included in the control circuit 152, and reference numeral 156 denotes the level shift circuit shown in Fig. 4. Data latch parts 265 represent the input register circuit 154 and the storage register circuit 155 that are shown in Fig. 4. In addition, decoder parts (gray scale voltage selection circuits) 261, amplifier circuit pairs 263, and switching parts ~~(2)~~ 267, 264 for switching the outputs of the amplifier circuit pairs 263 constitute the output circuit 157 shown in Fig. 4.

In this construction, a first switching part ~~(1)~~ 262 and the second switching parts ~~(2)~~ 264 are controlled on the basis of the alternation signal M in Fig. 4

Symbols Y1, Y2, Y3, Y4, Y5 and Y6 denote, respectively, the first, second, third, fourth, fifth and sixth drain signal lines D.

In the drain driver 130 shown in Fig. 5, the first switching part ~~(1)~~ 262 switches data acquiring signals to be inputted to the data latch parts 265 (more specifically, the input register circuit 154 shown in Fig. 4), thereby inputting display data for each color to the corresponding pair of adjacent ones of the data latch parts 265 for each color.

Each of the decoder parts 261 is made of a high voltage decoder circuit 278 and a low voltage decoder circuit 279. The high voltage decoder circuit 278 selects a gray scale voltage of positive polarity corresponding to the display data outputted from the corresponding one of the data latch parts

In the dot inversion method, the gray scale voltage for each color is of opposite polarity to the gray scale voltage for the adjacent color, and the arrangement of the high voltage decoder circuits 271 and the low voltage decoder circuits 272 of the amplifier circuit pairs 263 is in the order of the high voltage amplifier circuit 271 → the low voltage amplifier circuit 272 → the high voltage amplifier circuit 271 → the low voltage amplifier circuit 272. Data acquiring signals to be inputted to the data latch parts 265 are switched by the first switching part ~~(1)~~ 262, thereby inputting display data for each color to the corresponding pair of adjacent ones of the data latch parts 265 for each color, and according to this input operation, the output voltages from the high voltage amplifier circuits 271 or the low voltage amplifier circuits 272 are switched by the second switching part ~~(2)~~ 264 and are outputted to the drain signal lines D to which to output gray scale voltages for the respective colors, for example, to the first drain signal line Y1 and the fourth drain signal line Y4. In this manner, a gray scale voltage of positive polarity or negative polarity can be outputted to each of the drain signal lines D.

Fig. 6A is a block diagram showing transmission paths of display data from the display control device 110 to the liquid crystal display panel 10 shown in Fig. 1, Fig. 6B is an eye-diagram explaining the arrangement of the display data outputted from the display control device, and Fig. 6C is waveform diagrams explaining the phase relationship between